WEST Search History

DATE: Wednesday, August 27, 2003

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT,JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L13	((pre adj crusor$) near3 equaliz$3) and ((post adj crusor$) near3 equaliz$3) and ((isi) or (intersymbol adj interference$))	0	L13
L12	((pre adj crusor$) near3 equaliz$3) same ((post adj crusor$) neaR3 equaliz$3) same ((isi) or (intersymbol adj interference$))	0	L12
L11	(tail near2 (bit$ or symbol$ or signal)) and ((head or leading) near2 (symbol$ or bit$ or signal$)) and equaliz$3	34	L11
L10	(tail near2 (bit$ or symbol$ or signal)) same ((head or leading) near2 (symbol$ or bit$ or signal$)) same equaliz$3	0	L10
L9	(tail near2 (bit$ or symbol$ or signal)) same (head or leading (symbol$ or bit$ or signal$)) same equaliz$3	55	L9
L8	((filter$3 or equaliz$3) same (tail$)) and ((filter$3 or equaliz$3) near4 (head$)) and ((isi) or (intersymbol adj interference$))	25	L8
L7	((filter$3 or equaliz$3) same (more or most) near4 significant$) and ((filter$3 or equaliz$3) near4 (less or least or last) same (significant$)) and ((isi) or (intersymbol adj interference$))	0	L7
L6	((filter$3 or equaliz$3) same (more or most) near4 significant$) and ((filter$3 or equaliz$3) near4 (less or least or last) same (significat$)) and ((isi) or (intersymbol adj interference$))	0	L6
L5	((filter$3 or equaliz$3) with (more or most) near significant$) and ((filter$3 or equaliz$3) with (less or least or last) with (significat$)) and ((isi) or (intersymbol adj interference$))	0	L5
L4	((filter$3 or equaliz$3) near3 (more or most) near significant$) and ((filter$3 or equaliz$3) near3 (less or least or last) near3 (significat$)) and ((isi) or (intersymbol adj interference$))	0	L4
L3	((filter$3 or equaliz$3) near3 (more or most) near significant$) and ((filter$3 or equaliz$3) near3 (less or least or last) near3 (significat$)) and ((isi) or (intersymbol adj interference$)) and ((multiple or pulrality) near3 algorithm$)	0	L3
L2	((filter$3 or equaliz$3) near3 (more or most) near significant$) same ((filter$3 or equaliz$3) near3 (less or least or last) near3 (significat$)) same ((isi) or (intersymbol adj interference$)) same ((multiple or pulrality) near3 algorithm$)	0	L2
L1	((filter$3 or equaliz$3) near3 ((more or most) near significant$) near3 (less or least or last)) near3 ((isi) or (intersymbol adj interference$)) near5 ((multiple or pulrality) near3 algorithm$)	0	L1

END OF SEARCH HISTORY

L8: Entry 4 of 25 File: USPT Aug 20, 2002

DOCUMENT-IDENTIFIER: US 6437932 B1
TITLE: Decision based time-varying equalizers

Brief Summary Text (6):
The growing demand for digital storage capacity has also prompted an interest in the use of digital signal processing methods as a means of continuing increases in density. The general similarity of read and write processes in disk and tape drive units to data detection in transmission and communication systems has focussed interest on the application of equalization and coding methods to channels for both tape and disk drive systems. In particular, read channels have received special attention because the information has to be processed faster. Equalizers are used in both tape and disk drive read channels. In particular, decision feedback equalizers have been used to recover digital signals in read channels. Two types of noise dominate magnetic recording and read channels. One is regular noise caused, by thermal noise in electronics and random variations in the magnetic media. The other type of noise is intersymbol interference (ISI). Regular noise is found everywhere and effects all channels. ISI becomes worse with increasing density. Pulses generated by transitions in the magnetic media tend to overlap as transitions become closer with higher recording densities. Many of these decision feedback equalizers incorporate finite impulse response (FIR) filters to reduce errors caused by interference between successive pulses of data. This interference is also known as intersymbol interference (ISI). Additionally, errors may occur when the peas of positive and negative pulses do not have the same magnitude.

Brief Summary Text (7):
Presently available equalizers used in read channels contain coefficients that are determined to reduce errors in data transmission (e.g., ISI). The presently available adaptive equalizers adapt or alter coefficients based on an error signal derived from errors in the output of the read channel. These equalizer coefficients, however, are not optimal for all possible types of data patterns. Therefore, it would be advantageous to have an improved apparatus for equalizing signals to reduce errors in transmission of data.

Detailed Description Text (2):
With reference now to the figures, and in particular with reference to FIG. 1, a block diagram of a decision feedback equalizer (DFE) 100 is depicted in accordance with a preferred embodiment of the present invention. DFE 100 includes a forward equalizer 102, a backward equalizer 104, a summing circuit 106, and a symbol detector 108, such as, for example, a slicer. DFE 100 is used for suppressing inter-symbol interference (ISI) in high density magnetic recording, according to the present invention. Forward equalizer 102 receives an analog input waveform according to the present invention. Forward equalizer 102 filters the signal based on prior data patterns in accordance with a preferred embodiment of the present invention. The filtered signal is sent to summing circuit 106, which sums the signal from forward equalizer 102 and from backward equalizer 104 to produce a summed signal. Backward equalizer 104 modifies the signal by subtracting the trailing edges of pulses in the waveform in accordance with a preferred embodiment of the present invention. Often times the trailing edges of a positive pulse and a negative pulse are different. Slicer 108 produces a best estimate of the data symbol, given an input from summing circuit 106.

Detailed Description Text (7):
With reference now to FIGS. 2A-2D, more detailed block diagrams of DFEs are depicted in accordance with a preferred embodiment of the present invention. According to the present invention the forward equalizers (e.g., a filter bank containing FIR filters

or a single FIR filter connected to a memory containing different sets of coefficients) are employed to sharpen the leading edges of pulses based on a data pattern, such as a series of logic zeros followed by a logic one or on the expected polarity of the next pulse. The backward equalizer cancels tails based on the polarity of the pulses according to the present invention. The backward equalizer detects the polarity of the pulse and knows that the trailing edge will interfere with the next pulse and the proper set of coefficients is selected to cancel the trailing edge to eliminate interference according to the present invention. DFE 300 in FIG. 2A includes a filter bank 302 containing FIR filters 304, 306, and 308 according to the present invention. The output of FIR filters 304, 306, and 308 in filter bank 302 are connected to summing circuit 304 with the output of summing circuit 304 being connected to slicer 306. DFE 300 also includes a backward equalizer 308 with the output bits from slicer 306 used as an input into backward equalizer 308 as in a conventional DFE. Additionally, the data bits from slicer 306 are directed into selection logic 310, which selects one of FIR filters 304, 306, or 308 in filter bank 302 based on the data output from slicer 306 according to the present invention. In this manner, the best FIR filter in filter bank 302 may be selected for a given prior data pattern for different symbol decisions generated by slicer 308 to minimize data errors caused by a particular data pattern according to the present invention.

Detailed Description Text (11):
Feedback cancellation terms for cancelling ISI caused by positive and negative pulses having different peak magnitudes may be implemented within an FIR filter 318 in DFE 320 in FIG. 2C as coefficients according to the present invention. Different sets of coefficients are used to provide feedback cancellation terms, depending on the polarity and magnitude of the pulse whose ISI is being cancelled. These coefficients are stored within coefficient memory 322 and are designed to cancel tails caused by a positive and a negative pulse having different peak magnitudes according to the present invention. The particular sets of coefficients used by FIR filter 318 are selected by selection logic 310 based on the output from slicer 306.

Detailed Description Text (12):
Alternatively, the FIR filter 318 may be implemented in DFE 324 in FIG. 2D using a filter bank 326 according to the present invention. Filter bank 326 includes FIR filter 328 and FIR filter 330, which have their outputs connected to summing circuit 304. The output of slicer 306 is routed to FIR filter 328 or FIR filter 330, based on pulse polarity, using separator 332. If the output of slicer 306 is being directed to FIR filter 328, a zero is being directed to FIR filter 330, and vice versa. FIR filter 328 and FIR filter 330 each contain coefficients that result in positive and negative pulses canceling to eliminate the occurrence of tails. In this manner, the presently claimed invention reduces data errors.

Detailed Description Text (18):
Manufacturing variation is one cause of MR head nonlinearities. Thus, a disk drive with several MR heads may contain several different types of nonlinearity. In such a situation, several sets of FIR filter coefficients can be used and chosen based on prior data and on the particular MR head being used. The coefficients may be determined through a training sequence performed during manufacturing or on power up to generate the filter coefficients for use with each individual MR head. Additionally, different coefficients may be used for each head in a multi-head drive system.

Other Reference Publication (2):
"An Adaptive DFE for Storage Channels Suffering for Nonlinear ISI", pp. 1638-1642,13 Author(s) Fisher et al., World Prosperity Through Communications, Boston, Jun. 11-14, 1989, vol. 3, IEEE.

L8: Entry 5 of 25 File: USPT Jul 24, 2001

DOCUMENT-IDENTIFIER: US 6266350 B1
TITLE: Off-line broadband network interface

Detailed Description Text (3):
According to the present invention, the signal processing required for receiving or transmitting a bit data stream from a shared medium is accomplished by a processor independent of the network interface. FIG. 3 shows a network interface 300 according to this invention. Network interface 300 interfaces a host station 350 to a shared medium 400. Shared medium 400 may physically be one of several media capable of carrying signals, including copper twisted-pair, coaxial cable, power lines, optical cable, wireless RF and wireless IR. Shared medium 400 supports a multiple access protocol such as Ethernet. In addition, embodiments of this invention are applicable to unconditioned wiring on the shared medium that can result in severe channel distortion. The nature of the channel distortion will generally be different for each pair of stations on the network, therefore equalization parameters will be different for each path on the network, i.e., there is generally a different set of equalization parameters for every pair of stations. Equalization parameters and equalizer training is discussed in a later section of this document (see the Channel Estimation, Equalizer Training, and Header Processing section).

Detailed Description Text (13):
A typical network may have several stations, so it is possible that only a small percentage of the data packets will be intended for a given station. In those embodiments that perform equalization training on each received data packet, it is highly beneficial for host station 350 to avoid training its receiver on packets not intended for that station. This requires that the receiver determine whether or not a packet is intended for host station 350 before the signal processing of payload data 2104 or header information 2103. A further discussion of packet recognition, timing synchronization and equalizer training is given later in this document (see Channel Estimation, Equalizer Training, and Header Processing).

Detailed Description Text (19):
The method consists of two steps. First, a channel estimate is constructed from a training sequence in the preamble of the received signal. Although a channel estimate may have previously been determined for the channel, determining a channel estimate on every incoming data packet sensitizes host station 350 to different channel distortions over different paths. A discussion of estimating channels is given in a separate section, Channel Estimation, Equalizer Training and Header Processing. In the second step, for each destination address of interest to host station, the channel estimate is convolved with the encoded destination address and the result is compared to the appropriate portion of the received data packet. If the difference between the result and the received data packet is below a threshold value then a match has occurred. If there is no match, then the data packet can be ignored and discarded. The process of convolving the channel estimate with the destination address of interest involves only additions, making the process especially suitable for efficient hardware implementation. In most embodiments, however, the method is implemented in off-line processor 351.

Detailed Description Text (30):
MAC controller 206 receives signal CS from carrier sense/header filter 302 and signal CD from collision detect 204 and controls the timing of transmitting data to shared medium 400 by controlling the throughput of gated TX CODEC 305. When a data collision is detected by collision detect 204 or a data packet is sensed by carrier sense/header detect 302, MAC controller 206 prevents gated TX CODEC 305 from processing data packets from TX Queue 208. Hybrid 209, therefore, is prevented from

transmitting data onto shared medium 400.

Detailed Description Text (31):
FIG. 5 shows an embodiment of the invention capable of connecting to several shared media such as a local and a wide area network shared medium or of using different frequency bands on the same shared medium. In FIG. 5, network interface components hybrid 209, gated RX CODEC 303, carrier sense/header filter 302, gated TX CODEC 305, MAC 206, and collision detect 204 are instantiated in multiple copies. Each of the multiple copies is connected to a different shared medium 530 or use different frequencies on the same shared medium 530. In FIG. 5, the multiple copies include a transmit/receive 510 and a transmit/receive 511 that are connected to shared media 531 and 532, respectively. In general, any number of transmit/receive multiple copies are possible. A Multi-RX Queue receives sample packets from all of the multiple copies (including transmit receive 510 and 511 as well as gated CODEC 303), stores them, and transmits them to the host processor 510 of station 520. A Multi-TX Queue 508 holds transmit packets destined for all of shared media 530, 531, and 532 and transmits the transmit packets to the corresponding a gated TX CODEC (gated CODEC 305 or its counterpart in transmit/receive 510 or 511). The transmit packet and the sample packets are interleaved in the queues, each of the transmit packets and received packets having an identifier that identifies which shared medium 530, 531, or 532 that the packet is associated with.

Detailed Description Text (40):
In an alternative embodiment, the equalizer coefficients computed by header processor 701 are made such that the function of adjustment for baud phase offset of resampler 702 and the function of receive filter 707 are accomplished in the FFE 704.

Detailed Description Text (42):
In the preferred embodiment shown in FIG. 7, correction for intersymbol interference, a result of dispersion in the channel, is accomplished by a decision feedback equalizer comprising feed-forward equalizer 704 and feed-back equalizer (DFE) 705. In other embodiments, equalization may be accomplished by alternative methods including a decision feed-back equalizer having no feed-forward section or a linear equalizer having no feed-back section. The parameters of feed-forward equalizer 704 and feed-back equalizer 705 are adaptively chosen in adapter 712 in order that the removal of intersymbol interference by the equalizer is optimized. The equalizer outputs a corrected data signal.

Detailed Description Text (57):
FIG. 15 shows a block diagram of modulator 1405. Modulator 1405 includes a scrambler 1501, a bit mapper 1502, a trellis encoder 1503, a precoder 1504, a transmit filter 1506, and a header generator 1505. Precoder 1504 is optional and the host data is either processed through bit mapper 1502 or trellis encoder 1503 depending on parameters input to modulator 1405 from path 1404.

Detailed Description Text (58):
Channel Estimation, Equalizer Training, and Header Processing

Detailed Description Text (72):
As an alternative to linear equalization, the header may be precoded at the transmitting station. (See G. D. Forney, Jr., and M. V. Eyuboglu, "Combined Equalization and Coding Using Precoding, IEEE COMM. MAG., December 1991, at 25-34). Precoding is a non-linear equalization method with near-optimal signal to noise performance. There are several different types of preceding that may be used but Tomlinson Precoding is probably the simplest and is appropriate equalizing the header.

Detailed Description Text (76):
In this method, preamble 2102 comprises two tones separated in frequency by one-fourth the baud rate. Other separations of the two tones are possible. The two tones are linearly equalized at the transmitter to correct the channel distortion for a single destination. The resulting preamble, therefore, has length of about 28 symbols, including tails from the linear equalization. At higher baud rates (e.g. 10 Mbaud) the preamble may need to be lengthened.

WEST Search History

DATE: Wednesday, August 27, 2003

Set Name side by side	Query	Hit Count	Set Name result set
	DB=USPT,JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=OR		
L8	((filter$3 or equaliz$3) same (tail$)) and ((filter$3 or equaliz$3) near4 (head$)) and ((isi) or (intersymbol adj interference$))	25	L8
L7	((filter$3 or equaliz$3) same (more or most) near4 significant$) and ((filter$3 or equaliz$3) near4 (less or least or last) same (significant$)) and ((isi) or (intersymbol adj interference$))	0	L7
L6	((filter$3 or equaliz$3) same (more or most) near4 significant$) and ((filter$3 or equaliz$3) near4 (less or least or last) same (significat$)) and ((isi) or (intersymbol adj interference$))	0	L6
L5	((filter$3 or equaliz$3) with (more or most) near significant$) and ((filter$3 or equaliz$3) with (less or least or last) with (significat$)) and ((isi) or (intersymbol adj interference$))	0	L5
L4	((filter$3 or equaliz$3) near3 (more or most) near significant$) and ((filter$3 or equaliz$3) near3 (less or least or last) near3 (significat$)) and ((isi) or (intersymbol adj interference$))	0	L4
L3	((filter$3 or equaliz$3) near3 (more or most) near significant$) and ((filter$3 or equaliz$3) near3 (less or least or last) near3 (significat$)) and ((isi) or (intersymbol adj interference$)) and ((multiple or pulrality) near3 algorithm$)	0	L3
L2	((filter$3 or equaliz$3) near3 (more or most) near significant$) same ((filter$3 or equaliz$3) near3 (less or least or last) near3 (significat$)) same ((isi) or (intersymbol adj interference$)) same ((multiple or pulrality) near3 algorithm$)	0	L2
L1	((filter$3 or equaliz$3) near3 ((more or most) near significant$) near3 (less or least or last)) near3 ((isi) or (intersymbol adj interference$)) near5 ((multiple or pulrality) near3 algorithm$)	0	L1

END OF SEARCH HISTORY

L8: Entry 8 of 25 File: USPT Oct 31, 2000

DOCUMENT-IDENTIFIER: US 6141783 A
TITLE: Error propagation limiting encoder/decoder for multilevel decision feedback equalization

Brief Summary Text (4):
Decision Feedback Equalization (DFE) is a well-known scheme used to detect signals transmitted across communications and recording channels with intersymbol interference. In DFE, a forward equalizer shapes the readback pulse in a desired way and a feedback equalizer attempts to cancel the

Brief Summary Text (5):
intersymbol interference. However, a problem arises with DFE, in that the feedback mechanism has the potential to cause long bursts of errors.

Brief Summary Text (6):
The version of DFE called Multilevel Decision Feedback Equalization (MDFE), described by J. G. Kenney, L. R. Carley and R. Wood in the article "Multi-level Decision Feedback Equalization for Saturation Recording," EEE Transaction on Magnetics, vol. 19, no. 4, pp. 2160-71, July 1993, has several advantages when used in magnetic recording. In MDFE, the channel is equalized into a linear channel on non-return to zero (NRZ) (i.e. .+-.1) sequences defined by dibit response with a main lobe of positive taps a.sub.0, a.sub.1, a.sub.2 and a tail of negative taps -a.sub.3, -a.sub.4, -a.sub.5, . . . , -a.sub.L. The feedback equalizer attempts to cancel the negative taps. According to the formulation by J. L. Kenney and C. M. Melas in the article "Pipelining for Speed Doubling in MDFE," Conference Proceedings of the ICC '96, it is required that a.sub.1 >a.sub.0 =a.sub.2, yielding signal levels .+-.(a.sub.1 +2a.sub.0), .+-.a.sub.1, .+-.(a.sub.1 -2a.sub.0). After cancellation, a threshold detector, with threshold =0, makes the bit decision. This would not work if the lowest level, a.sub.1 -2a.sub.0, were very small or negative, so the data sequences are constrained to eliminate that level. This is accomplished by imposing a d=1 run length limited constraint (which forbids the NRZ patterns 1 -1 1 and -1 1 -1). An upper run length limit is also imposed for purposes of timing control. Typically a standard rate 2:3 (d, k)=(1, 7) run length code is used.

Detailed Description Text (5):
A data recovery circuit 6 with multi-level decision feedback equalization (MDFE), according to the present invention, is shown in FIG. 1b. Such a circuit is typically used to recover data from a magnetic media or a communication channel. In a preferred embodiment, the circuit is used in a hard disk drive. The analog signal from the read head is filtered by analog filter 102. The filtered analog signal is then applied to digital detection channel 104. Digital detection channel 104 includes an analog to digital converter (ADC) 106, a forward equalizer 108, threshold detector 110, decoder 112 and feedback equalizer 114. ADC 106 samples the analog read signal at timing intervals defined by sample clock signal 116. The sampled read signal for digital detection channel 104 is equalized by forward equalizer 108. The binary data is detected by the threshold detector, 110 and input to decoder 112, which generates the final output data from the read circuit.

Detailed Description Text (6):
The forward equalizer 108 shapes the readback pulse response to a desired form, striking a compromise among preserving signal energy, limiting intersymbol interference and mitigating noise boost. Denote the pulse response by

L11: Entry 24 of 34 File: USPT Apr 21, 1998

DOCUMENT-IDENTIFIER: US 5742642 A
TITLE: Signal processing method and apparatus for reducing equalizer error

Abstract Text (1):
A decision feedback equalizer (DFE) is controlled co equalize a current signal sample for intersymbol interference and/or other distortion caused by the communications channel. An incorrect symbol decision by the DFE is detected and corrected to prevent propagation of the error with possible adverse effects on subsequent DFE decisions. More specifically, an error threshold is determined based on an expected bit error rate and a first postcursor value h sub.1 of the communications channel impulse response. The decision feedback equalizer determines an intersymbol interference (ISI) component in a first, current sample of the signal being processed. The ISI component is subtracted from the current sample to generate an equalized sample. A corresponding symbol value is detected using that equalized sample. A symbol error is calculated by subtracting the equalized sample from the detected symbol value. The symbol error is compared with the error threshold. If the magnitude of the symbol error is less than the equalizer error threshold, the probability of a symbol decision error is low, and no preventive or corrective action is taken. However, if the magnitude of the symbol error is greater than the error threshold, a temporary symbol value is generated in place of the detected symbol value. The next, second sample is received and its corresponding symbol value is detected using this temporary symbol value. The second symbol error resulting from the use of the temporary symbol value is then determined. Using that second symbol error, a corrected, final symbol value is determined for the first sample that ensures symbol decision errors are not propagated through the DFE.

Brief Summary Text (2):
The invention relates to decision feedback equalizers, and more particularly, to decision error propagation through a decision feedback equalizer.

Brief Summary Text (4):
Equalizers are commonly used in digital communication systems where digital symbols are transmitted from a digital transmitter over a communications channel and received at a digital receiver. Transmission of coded binary data requires symbol synchronization at the digital data receiver. In general, the receiver clock of a receiving transceiver interface are adjusted to track and compensate for frequency drift between the oscillators used in the transmitter located at the opposite end of the communications loop as well as to track and compensate for changes in the transmission media. Digital receivers rely on signal processing to recover the transmitted digital information. The received signal is sampled at discrete time intervals and converted to its digital representation. A timing recovery function synchronizes the receiver clock so that received symbols can be sampled at an appropriate sampling instance to determine their correct values, (e.g., an optimum sampling instance would be at the peak of the sampled pulse or pulse amplitude modulated (PAM) codes). This task is complicated, however, because the received pulses are distorted.

Brief Summary Text (5):
One source of disturbance is echoes from transmitted pulses from the transmitting portion of the receiver coupled across a hybrid circuit and detected at the receiver input. Such transmit pulse echoes are typically removed by an echo canceller, e.g., a transversal filter which models the signal and subtracts it from the received signal. But even after the echo canceller removes the echoes of transmitted pulses, the received pulses are still distorted as a result of the transmission path characteristics, e.g., attenuated, and most significantly, intersymbol interference

(ISI) is introduced. The result is that relatively square, narrow, transmitted pulses are "smeared," i.e., distorted and widened, by the time they are received. More particularly, the "tail" of one symbol pulse extends into the time period of the next transmitted symbol pulse making it difficult to determine the correct amplitude of the pulse actually transmitted during the symbol period. Another factor is that the communications channel is not usually known initially--at least not precisely. Even if the channel is known initially, it may change with time. Therefore, the varying channel conditions must be monitored closely during transmission.

Brief Summary Text (6):
The general process of correcting the channel induced distortion is called equalization. Decision feedback equalizers are used (as explained more fully below) to suppress intersymbol interference caused by the "tails" of previously transmitted symbols according to the continuously estimated impulse response of the communications channel.

Brief Summary Text (8):
In practice, a feedback equalizer filter for compensating for ISI at the receiver contains various parameters, e.g., digital filter taps or coefficients, that are adjusted on the basis of estimated channel characteristics. A common choice for an equalizer feedback filter is a transversal filter such as that shown in FIG. 1. A transversal filter is essentially a delay line with several delays z.sup.-1, where delay z.sup.-1 corresponds in a digital communications application to the symbol duration. The tap coefficients, C.sub.n, are set to subtract the effects of interference from symbols that are adjacent in time to the desired symbol. The criteria for selecting or adjusting the C.sub.n coefficients is typically based on the minimization of either peak distortion or mean squared distortion. A preferred approach employs a least mean squares (LMS) algorithm to adjust the coefficients.

Brief Summary Text (10):
Decision feedback equalization uses previous symbol decisions, combined with the knowledge of the channel response, to form an estimate of the intersymbol interference at the current symbol decision instant due to previously transmitted symbols. This estimate is then subtracted from the received signal with the hope of reducing the influence of ISI in the decision value. If the previous equalizer decisions are all correct and the channel response is known perfectly, the ISI caused by previously detected symbols would be eliminated entirely. Unfortunately, this ideal situation is rarely if ever achieved.

Brief Summary Text (11):
Reference is now made to the decision feedback equalizer (DFE) 10 shown in FIG. 2. The signal to be equalized, e.g., a received signal x.sub.k, filter 12 which attempts to model the ISI due to previously transmitted symbols. The transversal filter structure shown in FIG. 1 may be used to implement the feedback filter 12 in FIG. 2. The number of filter taps in the feedback filter 12 determines the number of previous symbol decisions which affect the current DFE decisions. The output r.sub.k of combiner 16 ideally should correspond to just the received signal for the current symbol. Detector 14 detects the value of the symbol that best corresponds to r.sub.k to generate a detected symbol signal .alpha..sub.k. A difference between the input to the detector r.sub.k and the output of the detector .alpha..sub.k is determined in combiner 18 to generate a symbol error .epsilon..sub.k. Again, in an ideal system, this symbol error should essentially be zero.

Brief Summary Text (12):
Thus, a decision feedback equalizer operates by feeding back past data estimates or decisions. Unfortunately, these decisions may not correspond to the actual input data sequence, especially if the DFE has recently made decision errors. Because past decisions are used to cancel the ISI of the real data, DFE decision errors are likely "propagated" and may well lead to an "avalanche" of subsequent erroneous decisions. As a result of DFE error propagation, the postcursors of earlier symbols are (1) not eliminated by the DFE and (2) added to the current symbol estimate. Adding these DFE errors to the current DFE symbol estimate increases the likelihood of future decision errors in the DFE. The bottom line is that propagating DFE errors dramatically increase the bit error rate. Higher bit error rates may reduce the

communication system "throughput" with increasing numbers of erroneous data packets needing to be retransmitted.

Brief Summary Text (14):
IEEE Transactions on Communications, Vol. 37, No. 11, Nov. 1989, pp. 1126-1135, Rodney A. Kennedy et al., "Channels Leading to Rapid Error Recovery for Decision Feedback Equalizers"

Brief Summary Text (18):
IEEE Transactions on Communications, Vol. 42, No. 10, Oct. 1994, pp. 2786-2794, Norman C. Beaulieu, "Bounds on Recovery Times of Decision Feedback Equalizers"

Brief Summary Text (25):
The present invention provides a method for operating a decision feedback equalizer which equalizes the current signal sample for intersymbol interference caused by previous signal samples. An incorrect symbol decision by the DFE is detected and corrected to prevent propagation of the error with possible adverse effects on subsequent DFE decisions.

Brief Summary Text (26):
More specifically, an equalizer error threshold is determined based on the expected bit error rate and a first postcursor value h.sub.1 of the channel impulse response. The decision feedback equalizer determines an intersymbol interference component in a first current sample. The ISI component is subtracted from the current sample to generate an equalized sample. A corresponding symbol value is detected using that equalized sample. A symbol error is calculated by subtracting the equalized sample from the detected symbol value. The symbol error is compared with an error threshold. If the magnitude of the symbol error is less than the error threshold, the probability of an equalization error is low, and no preventive or corrective action is taken. However, if the magnitude of the symbol error is greater than the error threshold, a temporary symbol value is generated in place of the detected symbol value. The next, second sample is received, and its corresponding symbol value is detected using this temporary symbol value. The second symbol error resulting from the use of the temporary symbol value is then determined. Using that second symbol error, a corrected symbol value is determined for the first sample. The corrected symbol value ensures that DFE decision errors are not propagated. Choosing symbol decision thresholds as the temporary symbol values (rather than the symbol values themselves) guarantees in a noise free environment that decision errors will not propagate. This also maximizes the probability that decision errors will not propagate if noise is present.

Brief Summary Text (30):
While the present invention may advantageously be applied to digital communications systems, such as to the non-limiting ISDN transceiver example used below in the detailed description, the present invention has much wider general applicability. In particular, the present invention may be employed in equalizers in any application. A better understanding of the features and advantages of the present invention will be obtained by reference to the following detailed description of the invention and the accompanying drawings which set forth an illustrative, non-limiting embodiment in which the principles of the present invention are utilized.

Drawing Description Text (2):
FIG. 1 is a diagram of a transversal filter which may be used as the feedback filter in a decision feedback equalizer;

Drawing Description Text (3):
FIG. 2 is a function block diagram generally illustrating a decision feedback equalizer;

Detailed Description Text (9):
The digitized samples are filtered by a receive filter 50, the output of which is provided to summing block 52. Receive filter 50 increases the signal-to-noise ratio of the received signal by suppressing the "tail" of the received signal. The other input to summer 52 is an output from echo canceller 36. As described above, pulses transmitted onto subscriber loop 45 result in echo on the receiver side of the

hybrid 44 due to impedance mismatch. Unfortunately, it is difficult to separate the echoes of these transmitted pulses (using for example a filter) from the pulses being received from subscriber loop 45. Accordingly, echo canceller 36 generates a replica of the transmitted pulse waveform and subtracts it at summer 52 from the received pulses. The echo canceller is adjusted based upon an error signal between the received symbol and the detected symbol output at summer 66. Such an adaptive echo canceller is typically realized as a traversal, finite impulse response (FIR) filter whose impulse response is adapted to the impulse response of the echo path. The error is used to adjust the filter coefficients to "converge" the filter's response to the impulse response model of the communications channel.

Detailed Description Text (11):
The output of feedforward filter 56 x.sub.k from FIG. 4 is input to the combiner 58 which removes from signal x.sub.k the output of decision feedback equalizer 68. Decision feedback equalizer 68 receives as inputs a symbol error .epsilon..sub.k from differencer 66 and the detected symbol .alpha..sub.k generated by detector 60. The operation of the decision feedback equalizer 68 is described in further detail below. Symbols detected by detector 60 are decoded and descrambled in 2B1Q decoder 62 into scrambler 64, respectively, which perform the inverse operations of 2B1Q encoder 34 and scrambler 31. Ultimately the underlying data to be received is generated by descrambler 64.

Detailed Description Text (12):
As described above, the decision feedback equalizer uses past symbol decisions to synthesize and subtract from the current received signal sample x.sub.k an intersymbol interference (ISI) estimate ##EQU1## The symbol error .epsilon..sub.k can be mathematically described as the difference between the received signal sample x.sub.k, the ISI estimate d.sub.k, and a decision about the actual symbol value h.sub.0 .alpha..sub.k as follows: ##EQU2## The variables .alpha..sub.k and .alpha..sub.k are received data symbols and recovered data symbols, respectively; h.sub.i, and h.sub.i are the true and estimated values of the impulse response of the channel, respectively, where the estimated values of the channel impulse response (sometimes referred to as "cursors") are the DFE filter coefficients; (h.sub.i -h.sub.i) therefore is the corresponding error in the estimate of the channel impulse response; .eta..sub.k represents the external noise; and N is the number of taps in the DFE such as the DFE shown in FIG. 2. The pulse shape h.sub.i made up of precursors (h.sub.-1, h.sub.-2, h.sub.-3, . . .) and postcursors (h.sub.1, h.sub.2, h.sub.3, . . .) along with a main cursor h.sub.0 is generally not known because it results from an overall transfer function including the transmission medium, receive filter, etc. The sampled impulse response function is subsequently estimated using an adaptive finite impulse response (FIR) filter such as the transversal filter 12 in FIGS. 1 and 2. The sampled signal value at the current decision instant t.sub.k corresponds to the main cursor h.sub.0

Detailed Description Text (50):
Accordingly, the present invention advantageously improves the performance of any decision feedback equalizer by first identifying when an erroneous signal value decision has been made and then preventing propagation of that erroneous decision by correcting that decision. Thus, the first postcursor value along with the noise level are important factors in influencing the performance of the symbol decision error detection and analysis in accordance with the present invention. In application to high performance digital communication systems, the present invention provides significant improvement by reducing both bit error rate and the number of data packages which have to be retransmitted due to errors during reception.

Other Reference Publication (2):
IEEE Trans. Inform. Theory, vol. IT-20, pp. 490-497, Jul. 1974, D.L. Duttweiler, J.E. Mazo, and D.G. Messerschmitt, "An upper bound on the error probability in decision feedback equalizers".

Other Reference Publication (3):
IEEE Trans. Commun., vol. 37, No. 11, pp. 1126-1135, Nov. 1989, R.A. Kennedy, B.D.O. Anderson, and R.R. Bitmead, "Channels leading to rapid error recovery for decision feedback equalizers".

Other Reference Publication (4):
Electr. Lett., vol. 24, No. 17, pp. 1084-1085, 18 Aug. 1988, E. Dahlman and B. Gudmundson, "Performance improvement in decision feedback equalizers by using `soft decisions`".

Other Reference Publication (5):
IEEE J. Select. Areas Commun., vol. SAC-2, pp. 731-742, Sep. 1984, K. Wesolowski and J.G. Proakis, "A simplified two-stage equalizer with a reduced number of multiplications for data transmission over voiceband telephone links".

Other Reference Publication (9):
IEEE Trans. Commun., vol. COM-35, pp. 846-848, Aug. 1987, R.A. Kennedy and B.D.O. Anderson, "Error recovery of decision feedback equalizers on exponential impulse response channels".

Other Reference Publication (13):
IEEE Trans. Commun., vol. 42, No. 10, Oct. 1994, N.C. Beaulieu, "Bounds of recovery times of decision feedback equalizers".

CLAIMS:

1. A signal processing method for reducing an equalization error caused by a decision feedback equalizer (DFE) comprising the steps of:

(a) processing a received signal;

(b) determining an intersymbol interference component;

(c) subtracting from the received signal the intersymbol interference component to generate an equalized signal;

(d) deciding a current symbol value from the equalized signal;

(e) calculating a symbol error by subtracting the equalized signal from the decided symbol value;

(f) based on the symbol error, determining when the current value decision is erroneous; and

(g) preventing the erroneously decided current symbol value from adversely affecting subsequent symbol value decisions.

12. A signal processing method for processing symbol decisions made by a decision feedback equalizer (DFE) in detecting symbols corresponding to a series of signal samples received over a communications channel in a telecommunications system, comprising the steps of:

receiving a current signal sample;

determining in the decision feedback equalizer an intersymbol interference (ISI) component in the current sample;

subtracting from the current sample the intersymbol interference component to generate an equalized sample;

deciding a symbol value from the equalized sample; and

determining whether the symbol value was erroneously decided as a result of the decision feedback equalizer determining an incorrect intersymbol interference component.

14. The method in claim 12, further comprising:

if a magnitude of the a symbol error exceeds an error threshold, generating a temporary symbol value and using the temporary symbol value in place of the decided

symbol value to prevent propagation of the a symbol value decision error to subsequent symbol decisions made by the decision feedback equalizer.

18. A method for operating a decision feedback equalizer which equalizes a current signal sample for interference caused by other received symbols, comprising the steps of:

detecting when a decision error is made regarding the value decided for the current signal sample, and

preventing propagation of the decision error by the decision feedback equalizer in subsequent decisions made regarding the value of subsequent signal samples by correcting the erroneous decision including substituting a temporary value for the decided value.

21. The method in claim 18, wherein the detecting step includes:

setting an error threshold;

determining an equalizer error; and

comparing the equalizer error with the error threshold.

L11: Entry 30 of 34 File: USPT Apr 1, 1997

DOCUMENT-IDENTIFIER: US 5617450 A
TITLE: Digital subscriber loop interface unit

Abstract Text (1):
A digital subscriber loop interface unit, connected to a digital subscriber loop, includes an echo canceler for carrying out a echo canceling operation, a decision feedback equalizer for carrying out an equalizing operation, and a transversal filter, provided in at least one of the echo canceler and the decision feedback equalizer, in which a plurality of taps among all taps are grouped into groups, each group including a predetermined number of taps continuously arranged, a single tap coefficient being assigned to the taps in each group. A digital subscriber loop interface unit may include an echo canceler for carrying out a echo canceling operation by using a value obtained by adding +1 to a symbol value represented by a 2B1Q code. Further, the echo canceler may have a jitter echo canceler in which a convolution operation is carried out by using a value obtained by adding +1 to a symbol value represented by the 2B1Q code, the tap coefficient used in the convolution operation is changed in accordance with a time elapsing from occurrence of the jitter. Furthermore, a digital subscriber loop interface unit may have a low-pass filter in which a filter coefficient is changed based on whether the decision feedback equalizer is in or after a pull-in step.

Brief Summary Text (5):
In a case where a digital subscriber loop interface unit transmits digital signals represented by the 2B1Q codes using a twisted pair cable like an existing telephone subscriber loop, each transmission path code symbol is one of four values +3, +1, -1, and -3. In addition, for example, a baud rate of 80 kHz is selected as the transmission rate. In such a digital subscriber loop interface unit using the 2B1Q codes, it is required to effectively carry out an echo canceling process and an equalizing process for the input signals.

Brief Summary Text (6):
A conventional digital subscriber loop interface unit using the 2B1Q codes are formed, for example, as shown in FIG. 1. Referring to FIG. 1, the digital subscriber loop interface unit has a hybrid circuit (HYB) 102 connected to a subscriber loop 101, an analog-to-digital converter (A/D) 103, a high pass filter (HPF) 104, an AGC amplifier (AGC) 105, a low pass filter (LPF) 106, a decision feedback equalizer 109. The decision feedback equalizer 109 is formed of a discriminator (DEC) 107 and a transversal equalizer (EQL) 108. The digital subscriber also has a driver (DV) 110, an echo canceler 111 and a digital-to-analog converter (D/A) 115. The echo canceler 111 has a linear echo canceler (LEC) 112, a non-linear echo canceler (NEC) 113 and a jitter echo canceler (JEC) 114.

Brief Summary Text (8):
Echo components of the received signal is removed from the received signal by the echo canceler 111. The received signal is amplified by the AGC amplifier 105 so as to have a predetermined level and is supplied to the decision feedback equalizer (DFE) 109 via the low pass filter 106. The decision feedback equalizer (DFE) 102 removes inter-symbol interference from the received signal so that data is reproduced.

Brief Summary Text (9):
In a case where the AMI (Alternate Mark Inversion) codes which do not includes DC components are used as transmission codes, even if the hybrid circuit 102 is formed of a hybrid transformer cutting off the DC components, wave form distortion does not occur. On the other hand, in a case where the 2B1Q codes including DC components, if

the DC component is cut of the by the hybrid transformer of the hybrid circuit 102, the wave form distortion occurs. As a result, an impulse response shows a characteristic having a long tail. Thus, it is required to increase the number of taps of each of transversal filters in the echo canceler 111 and the decision feedback equalizer 109. In the transversal filter having a large number of taps, the size thereof is large and a large amount of processing is needed so that the dissipation power is increased.

Brief Summary Text (11):
Thus, as shown in FIG. 2, it has been known that a primary recursive filter (an IIR filter (Infinite Impulse Response filter)) 121 is added to the transversal filter. Referring to FIG. 2, the transversal filter has a plurality of delay elements (D), multipliers (.times.) and an adder (.SIGMA.) 120. Each of the delay elements (D) delays an input signal by a delay time corresponding to the baud rate. The primary recursive filter 121 has a adder (+), a multiplier (.times.) and a delay element (D). At respective taps each of which is between adjacent delay elements (D), symbols P(n)-P(n-M-1) sampled at sampling times n-(n-M-1) are obtained. The respective taps are connected to the multipliers (.times.), so that the multipliers (.times.) respectively multiplies the symbols P(n)-P(n-M) by tap coefficients CE.sub.1 -CE.sub.M. Multiplying signals output from the multipliers (.times.) are supplied to the adder (.SIGMA.) 120 and added to each other. The symbol P(n-M-1) sampled at the sampling time (n-M-1) and a tap coefficient CE.sub.M+1 are multiplied by the multiplier (.times.), and the multiplying signal is supplied to the primary recursive filter 121. An output signal of the primary recursive filter 121 is added to an adding output signal from the adder (.SIGMA.) 120 by an adder (+). A adding result at the adder (+) is obtained as an equalizing output signal y(n). The tap coefficient CE.sub.M+1 and an attenuation factor are supplied, as parameters, to the primary recursive filter 121. The attenuation factor corresponding to the long tail of the impulse response is equal to or greater than 0.95 and is less than 1.

Brief Summary Text (12):
FIG. 3 shows a unit in which an updating circuit for updating the tap coefficients to be supplied to the transversal filter is added to the circuit shown in FIG. 2. In FIG. 3, those parts which are the same those shown in FIG. 2 are given the same reference numbers. Referring to FIG. 3, an equalizing error signal k.multidot.e(n), obtained by multiplying an error signal e(n) at a sampling time n and a step size k, is supplied to the transversal filter. The symbol P(n) of the received signal at the sampling time n is successively delayed by the delay elements (D) serially connected to each other. The output signals at the respective taps each of which is between adjacent delay elements (D) are multiplied by the equalizing error signal k.multidot.e(n). Each of the multiplying signals is added to a tap coefficient delayed by one period of sampling time, and the adding result is multiplied, one of tap coefficient CE.sub.1 -CE.sub.M+1, by the signal at each tap.

Brief Summary Text (15):
FIG. 5 shows essential parts of a conventional decision feedback equalizer. Referring to FIG. 5, the decision feedback equalizer has a plurality of delay elements (D), an adder (.SIGMA.) 130, a discriminator 131, adders (+) and multipliers (.times.). Each of the delay elements (D) delays an input signal by a delay time corresponding to the baud rate. When a received signal x(n) is supplied to the decision feedback equalizer, the decision feedback equalizer outputs a received symbol P(n). An equalizing error signal e(n) is generated and the a feedback error signal k.multidot.e(n) is made by using the equalizing error signal e(n).

Brief Summary Text (16):
Received symbols P(n-1)-P(n-N) are respectively multiplied by tap coefficients Cd.sub.1 -Cd.sub.N, and the multiplying signals are added to each other by the adder 130. The adding result is output as an equaling signal y(n) from the adder 130. The equalizing signal y(n) is subtracted from the received signal x(n) so that the received signal x(n) is equalized. The equalized signal is supplied to the discriminator 131, and the discriminating result obtained by the discriminator 131 is used as the received symbol P(n). The decision feedback equalizer is applicable to various types of transmission apparatuses other than the digital subscriber loop interface unit.

Brief Summary Text (17):
In the decision feedback equalizer, a symbol value (A) is multiplied by a tap coefficient (B), and a number (C) is added to the multiplying result. In this case, one of values .+-.3 and .+-.1 is multiplied, as the symbol value (A), by the tap coefficient. Thus, the above calculating process can be carried out by using a 3-inputs adder and a shifter. In addition, it has been known that, in processes in a high pass filter and a low pass filter, a received signal having a plurality of bits and a filter coefficient are multiplied by each other using a shifting process in which the filter coefficient represented by an exponent of "2" is shifted.

Brief Summary Text (18):
In the decision feedback equalizer and the echo canceler in the digital subscriber loop interface unit, the total number of taps is fifty or more. A multiplying process and an adding process must be performed for each tap. Thus, the large number of processes is needed. To simplify processes, the following technique has been proposed (e.g. U.S. Pat. No. 4,926,472).

Brief Summary Text (20):
Essential parts of a conventional decision feedback equalizer using the "symbol value +1" are shown in FIG. 6. In FIG. 6, those parts which are the same as those shown in FIG. 5 are given the same reference numbers. Referring to FIG. 6, "1" is added to a received symbol P(n) which is discriminated by the discriminator 131 so that the symbol values .+-.3 and .+-.1 of the 2B1Q code is converted into symbol values 4, 2, 0 and -2. A DC (direct-current) correction part 132 corrects a difference between results of operations using the symbol values 4, 2, 0, and -2 obtained by adding +1 to the original symbol values .+-.3 and .+-.1 of the 2B1Q code and results of operations using the original symbol values of the 2B1Q, the operations including a convolution operation and an updating operation of the tap coefficients.

Brief Summary Text (21):
When a j-th tap coefficient, an equalizing error signal and a symbol value at a sampling time n are respectively represented by Cd.sub.j (n), e(n) and P(n), the j-th tap coefficient Cd.sub.j (n+1) at a sampling time (n+1) is represented as follows.

Brief Summary Text (33):
In the digital subscriber loop interface unit shown in FIG. 1, the low pass filter 106 at the front end of the decision feedback equalizer 109 forms a wave of post-cursor portion after the main pulse. Hereinafter the low pass filter 106 is referred to as a post-cursor equalizer. The transfer function of this post-cursor equalizer can be represented by

Brief Summary Text (35):
It can be determined, based on the gain of the AGC amplifier 105, whether or not the cable length is large or small. When the cable length is large, the received signal is attenuated. Thus, the AGC amplifier 105 amplifies the received signal with a large gain. On the other hand, when the cable length is small, the received signal is not almost attenuated, so that the AGC amplifier 105 amplifies the received signal with a small gain. Thus, in accordance with the gain of the AGC amplifier 105, the filter coefficient a of the post-cursor equalizer is changed. In a case where the above post-cursor equalizer is used, there is a problem in that a pull-in time (a time required to obtain a signal converging on a stable state) in a case of using a long cable may be greater than that in a case of using a short cable. Because the gain of the AGC amplifier is large in use of the long cable as has been described above, noise components are also enlarged so that a noise error becomes large, the pull-in time may be large.

Brief Summary Text (37):
The sampling phase is generally not constant at start of the pull-in operation, so that the optimum sampling phase is searched for by moving the sampling point in a time axis in the phase extracting circuit (not shown in figures). According to an algorithm of the decision feedback equalizer, the main-cursor (the main response) corresponds to an amplitude at a sampling time at which the maximum value is

obtained among a plurality of sampling values sampled every baud rate period T. The pre-cursor corresponds to an amplitude at a time previous by T to the sampling time at which the main-cursor is obtained. The sampling phase corresponding to the pre-cursor is normally determined at zero. The post-cursor corresponds to an amplitude at each of times delaying from the main-cursor by nT where n represents positive integers. For example, in FIG. 8(a) and (b), the pre-cursor is zero and sampling points a1 and b1 delaying from the precursor by the period T is the optimum phases for the pull-in process.

Brief Summary Text (40):
In concrete terms, in the case where the length of the cable is large, the frequency at which decision errors occur in initial step of the pull-in process in the decision feedback equalizer is lager than the frequency at which the decision errors occur in the case where the length of the cable is short. Thus, a long time is required to obtain right tap coefficients in the coefficient updating operation represented by the equation (1).

Brief Summary Text (41):
In the conventional digital subscriber loop interface unit formed as shown in FIG. 1, the 2B1Q code is used for the transmission of information. Since the hybrid circuit 102 is formed of the hybrid transformer, the transmission characteristic depends on the impedance of each of the hybrid transformers in both the transmitting side unit and the receiving side unit. Thus, even if the recursive filter is used, the number of taps of each of the echo canceler 111 and the decision feedback equalizer 109 must be twenty four or more. That is, the recursive filter is used only as aid.

Brief Summary Text (42):
In a subscriber side of the digital subscriber loop interface unit, after the pull-in process in the echo canceler 111 is completed by using the transmission signal to be transmitted to a destination, the taps of the echo canceler 111 are fixed. The pull-in process in the decision feedback equalizer 109 is then performed using the received signal. In the switching unit side, the transmission timing is fixed, so that the sampling phase must be synchronized with the timing of the received signal. Thus, the sneak time of the echo can not be fixed. As a result, in the pull-in process, the number of taps of both the echo canceler 111 and the decision feedback equalizer must be simultaneously updated.

Brief Summary Text (43):
In this case, if the tap coefficients are updated using the "symbol value +1" as the symbol in both the echo canceler 111 and the decision feedback equalizer 109, there is a case where the pull-in is incomplete. This is caused by using the same error in both the echo canceler 111 and the decision feedback equalizer 109. In general, each tap coefficient is calculated by based on the correlation between the symbol P(n-j) +1 and the error e(n) as indicated by the equation (1). In the echo canceler 111, the tap coefficients are obtained by using the transmission symbol, and in the decision feedback equalizer 109, the tap coefficients are obtained by using symbols reproduced from the received signals. That is, the tap coefficients are separately obtained in the echo canceler 111 and the decision feedback equalizer 109.

Brief Summary Text (44):
However, the value of the DC correction part indicated by the equation (2) depends on only the error e(n). When the pull-in processes in the echo canceler 111 and the decision feedback equalizer 109 are simultaneously performed using the same error e(n), the respective DC correction parts performs the same process. As a result, in the respective the echo canceler 111 and the decision feedback equalizer 109, the correction of DC components required by them are not always performed.

Brief Summary Text (45):
In addition, the echo canceler 111 has the non-linear echo canceler 113 which functions as the DC correction part. As a result, the echo canceler 111 may not be provided with the DC correction part. On the other hand, in the decision feedback equalizer 109, since the DC component are not ignored, the decision feedback equalizer 109 must be provided with the DC correction part for correcting the DC components.

Brief Summary Text (46):
As has been described above, in a case where both the echo canceler 111 and the decision feedback equalizer 109 carries out the convolution operation and the updating operation of the tap coefficient using the "symbol value +1", both the echo canceler 111 and the decision feedback equalizer 109 are in a state where there is substantially the DC correction part. Thus, in an initial state and/or in an step size, the tap coefficients are updated so that the non-linear echo canceler 113 corrects DC components which should be corrected by the DC correction part of the decision feedback equalizer 109. As a result, the tap coefficients reach limited value, and the non-linear echo canceler 113 can not perform the correction of non-linear components to be processed. In this case, the pull-in may be incomplete.

Brief Summary Text (47):
The tap coefficients of the transversal transformer of the decision feedback equalizer 109 correspond to the post-cursor portion of the impulse response, but the transversal transformer has no tap coefficients corresponding to the pre-cursor and the main-cursor. If the value of the DC correction part is limited to an item corresponding to the post-cursor (the value of the DC correction part is the sum of coefficients of only the post-cursor portion, and is close to "1" not close to zero.), the calculation of [(the value of the main-cursor).times.(the symbol value P(n)] must be performed when the error is calculated. As a result, the number of calculations can not be decreased.

Brief Summary Text (48):
If the term corresponding to the main-cursor is considered as the DC correction part, the value of the DC correction part is close to zero. In this case, the error e(n) is obtained in accordance with a calculation [(the main-cursor value Cd.sub.0).times.(the new symbol P(n)+1)]. As a result, the number of calculation is not increased. However, in this case, the control of the pull-in is complex. For example, before the pull-in of the tap coefficients in the decision feedback equalizer 109 is performed, the tap coefficient Cd.sub.0 corresponding to the main-cursor is calculated in a state where the tap coefficient corresponding to the post-cursor in the decision feedback equalizer 109 is maintained at zero. The AGC gain is then determined so that the calculated tap coefficient Cd.sub.0 falls within a predetermined range. If this AGC process is performed, since the coefficient value Cd.sub.0 corresponding to the main-cursor is not zero, the DC correction part can not be zero. The value of the DC correction part obtained when the AGC process is completed is approximately the same as the value of the main-cursor so as to be greatly different from zero. After this, the pull-in of the tap coefficient in the decision feedback equalizer 109 is performed. When the tap coefficient corresponding to the post-cursor is close to the final value, the DC correction part is gradually varied to a value close to zero.

Brief Summary Text (49):
As has been described above, the DC correction part in the decision feedback equalizer 109 has a large value once in the pull-in process, and is then varied so as to return to zero. Since the coefficient varies complexly as this, the step size must be filly controlled. As a result, the control is complex and the time required for the pull-in process is long.

Brief Summary Text (51):
The characteristics of the post-cursor equalizer (the low-pass filter 106) is selected so that the post-cursor portion of the impulse response, that is, the tail of the impulse response has a predetermined shape. Thus, if the cable is long, the emphasis of the high frequency components is insufficient so that the main pulse expands. As a result, the probability that an error occurs in the decision feedback equalizer 109 immediately after the pull-in process starts is increased, and the time required for the pull-in process is long.

Brief Summary Text (54):
The more specific object of the present invention is to provide a digital subscriber loop interface unit in which characteristics of the echo canceler and the decision feedback equalizer can be improved without substantially increasing the number of taps.

Brief Summary Text (55):
The above objects of the present invention are achieved by a digital subscriber loop interface unit connected to a digital subscriber loop, comprising: an echo canceler for carrying out a echo canceling operation; a decision feedback equalizer for carrying out an equalizing operation; and a transversal filter, provided in at least one of the echo canceler and the decision feedback equalizer, in which a plurality of taps among all taps are grouped into groups, each group including a predetermined number of taps continuously arranged, a single tap coefficient being assigned to the taps in each group.

Brief Summary Text (56):
According to the present invention, the characteristics of the echo canceler and the decision feedback equalizer can be improved without substantially increasing the number of taps.

Brief Summary Text (57):
The digital subscriber loop interface unit may comprise an echo canceler for carrying out a echo canceling operation by using a value obtained by adding +1 to a symbol value represented by a 2B1Q code; and a decision feedback equalizer for carrying out an equalizing operation.

Brief Summary Text (59):
In the digital subscriber loop interface unit, the decision feedback equalizer carries out the equalizing operation, in a pull-in step, by using a part of all the taps in which operation a symbol value represented by a 2B1Q code is used, and the decision feedback equalizer carries out the equalizing operation, after the pull-in step, by using all the taps in which operation a value obtained by adding +1 to a symbol value represented by the 2B1Q code.

Brief Summary Text (60):
According to the present invention, the pull-in step can be easily accomplished and the operation can be easily performed in the decision feedback equalizer.

Brief Summary Text (61):
The digital subscriber loop interface may comprise an echo canceler for carrying out an echo canceling operation; and a decision feedback equalizer for carrying out an equalizing operation, wherein the echo canceler has a jitter echo canceler for eliminating from a received signal echo components based on a jitter, the jitter echo canceler having: means for carrying out a convolution operation by using a value obtained by adding +1 to a symbol value represented by the 2B1Q code; means form changing the tap coefficient used in the convolution operation in accordance with a time elapsing from occurrence of the jitter; and a DC correction part to which "1" is always supplied and for changing a tap coefficient used therein in accordance with a time elapsing from occurrence of the jitter.

Brief Summary Text (63):
The digital subscriber loop interface may comprise an echo canceler for carrying out an echo canceling operation; a decision feedback equalizer for carrying out an equalizing operation; and a low-pass filter to which a signal processed by the echo canceler is supplied and for supplying a signal processed by the low-pass filter to the decision feedback equalizer, the low-pass filter having: means for changing a filter coefficient in accordance with a length of the digital subscriber loop; and means for changing the filter coefficient based on whether the decision feedback equalizer is in or after a pull-in step.

Brief Summary Text (64):
According to the present invention, even if the digital subscriber loop is long, the pull-in step can be easily accomplished in the decision feedback equalizer.

Drawing Description Text (6):
FIG. 5 is a diagram illustrating an essential part of a conventional decision feedback equalizer.

Drawing Description Text (15):

FIG. 13 is a diagram illustrating an essential part of a decision feedback equalizer provided in the digital subscriber loop interface unit according to a third embodiment of the present invention.

Drawing Description Text (16):
FIG. 14 is a diagram illustrating an essential part of a decision feedback equalizer provided in the digital subscriber loop interface unit according to a fourth embodiment of the present invention.

Drawing Description Text (17):
FIG. 15 is a diagram illustrating an S/N characteristic of a pull-in process carried out in the decision feedback equalizer according to the fourth embodiment.

Drawing Description Text (18):
FIG. 16 is a diagram illustrating a sampling phase characteristic of the pull-in process carried out in the decision feedback equalizer according to the fourth embodiment.

Detailed Description Text (3):
FIG. 9 shows a digital subscriber loop interface unit. Referring to FIG. 9, the digital subscriber loop interface unit has an echo canceler 1, a decision feedback equalizer 3 and a hybrid circuit connected to a digital subscriber loop 5. The digital subscriber loop interface performs transmitting and receiving information via the digital subscriber loop 5 by using the 2B1Q codes. The echo canceler 1 and the decision feedback equalizer 3 respectively have transversal filters (TRF) 6 and 7 in each of which respective symbols for a plurality of taps are multiplied by tap coefficients and multiplying results are added to each other. A plurality of taps which are at least a part of all the taps of a transversal filter of at least one of the echo canceler 1 and the decision feedback equalizer are grouped into groups so that each group includes a predetermined number of taps continuously arranged. The same tap coefficient is assigned to the taps in each group. The digital subscriber loop interface unit has also a high-pass filter (HPF) 8, a low-pass filter (LPF) 9, a controller 10, a driver 11, a digital-to-analog converter (D/A) 12 and an analog-to-digital converter 13.

Detailed Description Text (4):
In the above digital subscriber loop interface unit, the echo canceler 1 forms an echo replica used to cancel the echo of the transmission signal. The decision feedback equalizer 3 carries out the equalizing process so that the inter-symbol interference of the received signal is canceled. At this time, in taps corresponding to the tail portion of the transversal filter, the same tap coefficient is assigned to the taps in each group.

Detailed Description Text (9):
The digital subscriber loop interface unit has at least the echo canceler 1, the AGC amplifier 2, the decision feedback equalizer 3 and the hybrid circuit 4 connected to the digital subscriber loop 5 and transmits and receives information via the digital subscriber loop 5 by using the 2B1Q codes. In this digital subscriber loop unit, the echo canceler 1 may carry out an echo canceling process by using a value obtained by adding +1 to a symbol value represented by the 2B1Q code. The decision feedback equalizer 3 may perform, in a pull-in step, an equalizing process by using a part of the total number of taps and a symbol value represented by the 2B1Q code, and may perform, after the pull-in step, the equalizing process by using total number of taps and a value obtained by adding +1 to the symbol value represented by the 2B1Q code.

Detailed Description Text (10):
In the pull-in step, the decision feedback equalizer 3 uses symbols represented by the 2B1Q codes and uses a number of taps equal to or less than a number a half as many as the total number of taps. In this case, the process in the DC correction part can be omitted and the amount of operation can be decreased. After the pull-in step, the decision feedback equalizer 3 uses a value obtained by adding +1 to the symbol value and uses all the taps. At this time, the echo canceler 1 has been already in a stationary state. Thus, the tap coefficient in the non-linear echo canceler corresponding to the DC correction part is greatly slowly updated or the

updating operation is in a stop state. The decision feedback equalizer 3 pulls in essential taps including the main cursor, and the tap coefficient including the DC correction part is not irregularly and converges on a value to be corrected.

Detailed Description Text (11):
The digital subscriber loop interface unit has at least the echo canceler 1, the AGC amplifier 2, the decision feedback equalizer 3 and the hybrid circuit 4 connected to the digital subscriber loop 5 and transmits and receives information via the digital subscriber loop 5 by using the 2B1Q codes. In this digital subscriber loop interface unit, the echo canceler may have at least a jitter echo canceler for canceling echo components depending on jitter in which jitter echo canceler the convolution operation is performed by using a value obtained by adding +1 to the symbol value represented by the 2B1Q code. The echo canceler switches taps coefficients in accordance with a time elapsing from the generation of the jitter, and has a DC correction part, to which an input "1" is always supplied, for switching the taps in accordance with a time elapsing from the generation of the jitter.

Detailed Description Text (13):
The digital subscriber loop interface unit has at least the echo canceler 1, the AGC amplifier 2, the decision feedback equalizer 3, the hybrid circuit 4 connected to the digital subscriber loop 5, the wave shaping high-pass filter (HPF) 8 and the low-pass filter 9 in which filter coefficients are changeable, and transmits and receives information via the digital subscriber loop 5 using the 2B1Q codes. In this digital subscriber loop interface unit, the low-pass filter 9 may change the filter coefficient in accordance with the length of the digital subscriber loop 5, and may change the filter coefficient in accordance with whether the decision feedback equalizer 3 is in the pull-in step or after the pull-in step.

Detailed Description Text (14):
The low-pass filter changes the filter coefficient in accordance with gain of the AGC amplifier 2 so that the post-cursor characteristic of the impulse response is optimized. In the pull-in step in the decision feedback equalizer 3, the filter coefficient is changed so that the main response characteristic of the impulse response is controlled. That is, the filter coefficient is changed so that the pulse width of the main-cursor is decreased. According to this, the decision feedback equalizer 3 can rapidly carries out the pull-in process for obtaining the optimum a sampling phase. The changing of the filter coefficient may be performed by a sequential control in the controller 10.

Detailed Description Text (15):
In the above digital subscriber loop interface unit, the low-pass filter 9 may also change the filter coefficient by stages from starting the pull-in step in the decision feedback equalizer 3 to the end of the pull-in step.

Detailed Description Text (16):
In a case where the filter coefficient of the low-pass filter is changed, if the difference between the filter coefficient and the changed filter coefficient is large, there may be a case where the decision feedback equalizer 3 can not be changed to the last state under a condition in which the pull-in state is being maintained. When the filter coefficient is changed by stages, the difference between the filter coefficient and the changed filter coefficient in every stage is small. Thus, each tap coefficient of the decision feedback equalizer 3 can be converged to the right value under a condition in which the pull-in state is being always maintained.

Detailed Description Text (19):
A description will now be given, with reference to FIGS.10, 11A and 11B, of a first embodiment of the present invention. In the first embodiment, an essential part of the echo canceler 1 and/or the decision feedback equalizer 3 shown in FIG. 9 is formed as shown in FIG. 10.

Detailed Description Text (20):
Referring to FIG. 10, there are provided an adder 20 (.SIGMA.), a plurality of delay elements 21 (D), multipliers 22 (.times.) and adders 23. A received symbol P(n) is obtained at a sampling time n, and an equalizing output signal y(n) is obtained at

the sampling time n. Tap coefficients CE.sub.1 -CE.sub.M and CF.sub.1 -CF.sub.K are supplied to the multipliers 22.

Detailed Description Text (22):
Thus, the equalizing output signal y(n) is represented as follows. ##EQU1## In the above equation, .SIGMA..sup.M.sub.i=1 means an adding operation from i=1 to i=M, and .SIGMA..sup.K.sub.j=1 means an adding operation from j=1 to j=K.

Detailed Description Text (39):
The bit S2 located at the head of bits representing output data of the converting logic circuit 23c is equal to the sign bit S of the adding output data, and indicates a sign of a value represented by the exponent of "2". The bit S3 located at the tail end of the bits is equal to zero if the sign of a value in a bracket is the same as the sign in front of the bracket, and is equal to one if those signs differ from each other. In cases where the adding output data is .+-.9, .+-.5 and .+-.3, the bit S2 is zero, and in cases where the adding output data is .+-.7 and .+-.1, the bit S2 is one. In addition, in a case the adding output data is +9, the bit S3 is zero, and in a case where the adding output data is -9, the bit S3 is one. The two bits B1 and B2 indicates a pair of two numbers each of which is represented by the exponent of "2". That is, a pair (2.sup.3, 2.sup.0) is indicated by bits (1,1), a pair (2.sup.2, 2.sup.0) is indicated by bits (1,0), a pair (2.sup.1, 2.sup.0) is indicated by bits (0,1). Thus, the converting logic circuit 23c can be formed of a simple logic structure. In the multiplying operation in which a coefficient is multiplied by the output data of the converting logic circuit 23, the multiplying result is obtained by shifting the coefficient by a number represented by the two bits B1 and B2. The second term in each parentheses is always 2.sup.0 and the number of shifting bits corresponding to 2.sup.0 is zero.

Detailed Description Text (45):
A description will now be given, with reference to FIG. 13, of a third embodiment of the present invention. In FIG. 13, those parts which are the same as those shown in FIG. 12 are given the same reference numbers. Referring to FIG. 13, there are further provided a discriminator 27, adders 28 and 29 and a multiplier 30. This embodiment relates to the decision feedback equalizer 3 shown in FIG. 9. Thus, the input x(n) is a signal from which the echo components are eliminated by the echo canceler 1. The input x(n) and the output signal y(n) of this transversal filter are supplied to the adder 28 so that the difference between them is obtained. The difference value is supplied to the discriminator 27 and a discriminated symbol P(n) is output from the discriminator 27.

Detailed Description Text (47):
The estimation of the S/N ratio was carried out using the echo canceler 1 having a transversal filter in which M=18, L=3 and K=4 and the decision feedback equalizer 3 having a transversal filter in which M=16, L=3 and K=4. The following results were obtained.

Detailed Description Text (49):
In a case where the inductance of the hybrid transformer was 15 mH, the S/N of 22.35 dB was obtained. In this case, both the echo canceler 1 and the decision type feedback equalizer 3 were not provided with the recursive filter.

Detailed Description Text (50):
To obtain the above S/N ratio in the conventional structure, the transversal filter must have 24 taps and the recursive filter is needed. In this case, in view of the amount of processing, the equivalent number of taps of transversal filter is 26, because the primary recursive filter needs the same amount of processing as the transversal filter having two taps. On the other hand, in the above experiment, the echo canceler has 22 taps, the decision feedback equalizer 3 has 20 taps and the recursive filter is not needed. Thus, the equivalent number of taps of the traversal filter, in view of the amount of processing, can be decreased. That is, the amount of processing can be decreased, so that the dissipation power can be decreased.

Detailed Description Text (51):
A description will be given, with reference to FIG. 14, of a fourth embodiment of the present invention. This embodiment relates to the decision feedback equalizer 3

shown in FIG. 9. The echo canceler 1 uses a value represented by adding +1 to a symbol value. The decision feedback equalizer 3 decreases the number of taps in the pull-in step and uses a symbol value as it is. After the pull-in step, the decision feedback equalizer 3 increases the number of taps and uses a value represented by adding +1 to a symbol value. Referring to FIG. 14, there are provided delay elements 31 and 36, a discriminator 37 (DEC), adders 40A and 40B (.SIGMA.), a DC correction part 41, switches 43 and 44, multipliers 32, 34 and 46 (.times.) and adders 33, 35, 38, 39, 42 and 45 (+). Tap coefficients Cd.sub.0 -Cd.sub.N and Dd are supplied to the transversal filter shown in FIG. 14.

Detailed Description Text (53):
The output signal x(n) from the low pass filer 9 (see FIG. 9) is supplied to the adder 38 of the decision feedback equalizer 3, and the difference between the signal x(n) and the output signal y(n) of the transversal signal is obtained. The difference is supplied to the discriminator 37 and the symbol P(n) is output from the discriminator 37 as a discriminated output signal.

Detailed Description Text (59):
After the pull-in step in the decision feedback equalizer 3, the switch 43 is turned on and the switch 44 is switched from "0" to "1". As a result, the tap coefficient and other signals are obtained in accordance with the following equations.

Detailed Description Text (63):
In a range between 0 and 23,000 cycles, the pull-in step in the echo canceler was performed. In a range between 23,000 cycles and 30,500 cycles, the updating operation of the tap coefficients of the echo canceler was stopped and the pull-in step in the decision feedback equalizer was performed. In this case, the number of taps in the decision feedback equalizer 3 was eight and the updating operation of the tap coefficients and the convolution operation were carried out by using symbols having values .+-.3 and .+-.1 represented by the 2B1Q codes. After this, the number of taps was changed to twenty four and the updating operation of the tap coefficients and the convolution operation were carried out by using a value represented by adding +1 to a symbol value. In a range in which the number of cycles exceeds 35,000, the updating operation of the echo canceler taps is performed.

Detailed Description Text (64):
When the pull-in step was carried out under a condition in which the number of taps in the decision feedback equalizer 3 was eight, as shown in FIG. 16, although the residual was sightly large, a phase was pulled in the suitable sampling phase. After this, the phase was stably maintained at the sampling phase. That is, in a case where a value obtained by adding +1 to a symbol value was used, a problem in that it is difficult for the decision feedback equalizer to accomplish the pull-in of the phase was solved without increasing the amount of processing.

Detailed Description Text (81):
A description will now be given, with reference to FIG. 18, of a sixth embodiment of the present invention. Referring to FIG. 18, a digital subscriber loop interface unit has an echo canceler 61 (EC), an AGC amplifier 62 (AGC), a decision feedback equalizer 63, a hybrid circuit 64 (HYB) connected to a digital subscriber loop 65, a high-pass filter 68 (HPF), a low-pass filter 69 (LPF), a controller 70, a driver 71 (DV), a digital-to-analog converter 72 (D/A) and an analog-to-digital converter 73 (A/D). The low-pass filter 69 is formed of a delay element 74 (D), a factor unit 75 and an adder 76. The echo canceler 61, the decision feedback equalizer 63 and some units have the same structure as those in the previous embodiments, and duplicate description will be omitted.

Detailed Description Text (82):
The low-pass filter 69 formed of the delay element 74, the factor unit 75 and the adder 76 is a primary low-pass filter. A factor a of the factor unit 75 is controlled by the controller 70. The low-pass filter 69 corresponds to the post-cursor equalizer for equalizing the tail portion of the impulse response, as has been described above. The decision feedback equalizer 63 has, for example, 16 taps. Thus, the post-cursor can equalize a portion corresponding to only the 16 taps. In the decision feedback equalizer 63, to discontinue the error decision, the amplitude of the post-cursor should be equal to or less than a value a half as large

as the amplitude of the main-cursor.

Detailed Description Text (84):
Thus, the controller 70 controls the low-pass filter 69 in accordance with the gain information of the AGC amplifier 62 and the sequence from starting of the pull-in step so that the filter coefficient (the factor) a is set at a value corresponding to the length of the cable, and the filter coefficient a is changed from a time at which the pull-in step starts and to a time after the pull-in step. In a case where the cable is long, the impulse response is formed, for example, as shown in FIG. 8(a). In this case, due to selecting the filter coefficient a, the frequency characteristic is controlled so that the pulse width becomes narrow, as shown in FIG. 8(c). As a result, although the post-cursor becomes large to certain extent, the pull-in step can be easily accomplished in the decision feedback equalizer 63. In addition, after the pull-in step, the frequency characteristic is controlled so that the post-cursor has a required size.

Detailed Description Text (86):
When the filter coefficient a is changed as described above, in the decision feedback equalizer 63, the pull-in step is carried out again. In this case, the operation can follow the new filter coefficient within about 5,000 cycles. Thus, due to changing the filter coefficient when the state proceeds to the convergence and after convergence as described above, the excessive time corresponding to about 10,000 cycles is needed in comparison with the conventional system in which the filter coefficient set at start of the pull-in step is fixed. However, this excessive time is sufficiently shorter than the time corresponding to a few hundred thousands cycles needed in the pull-in step. In addition, since the main pulse width of the impulse response can be decreased as shown in FIG. 8(a) and (c), a case where the pull-in step is not accomplished does not occur.

Detailed Description Text (87):
In this embodiment, the low-pass filter 69 is connected to a back end of the AGC amplifier 62. However, since the low-pass filter 69 may be located between the echo canceler 61 and the decision feedback equalizer 63, the low-pass filter 69 may be connected to a front end of the AGC amplifier 62. In addition, the filter coefficient has a value of multiple of 0.125 (2.sup.-3). Thus, the multiplying operation of the filter coefficient can be carried out by the shifting operation. Further, the number of times the filter coefficient a is changed can be increased.

Detailed Description Text (88):
As has been described above, in the low-pass filter (the post-cursor equalizer) 69 for forming the post-cursor characteristic of the impulse response, the filter coefficient a is set at a value depending on the length of the cable, and is changed in accordance with the time elapsing from starting the pull-in step. Thus, the main pulse width of the impulse response can be decrease in the pull-in step, so that the pull-in step can be easily accomplished.

CLAIMS:

1. A digital subscriber loop interface unit connected to a digital subscriber loop, comprising:

an echo canceler for carrying out an echo canceling operation;

a decision feedback equalizer for carrying out an equalizing operation; and

a low-pass filter to which a signal processed by said echo canceler is supplied and for supplying a signal processed by said low-pass filter to said decision feedback equalizer, said low-pass filter having:

means for changing a filter coefficient in accordance with a length of said digital subscriber loop; and

means for changing the filter coefficient based on whether said decision feedback equalizer is in or after a pull-in step.